UTILITY PATENT APPLICATION TRANSMITTAL UNDER 37 C.F.R.§1.53(b)

ASSISTANT COMMISSIONER FOR PATENTS
Box PATENT APPLICATION
Washington D.C. 20231

Case Docket No.:P-035

Sir:

Transmitted herewith for filing is the patent application of
INVENTOR OR APPLICATION IDENTIFIER: Nam-Soo YEO, In-Tae KIM, Jong-Ho KIM and In-Hwan HWANG
FOR: PATH MANAGEMENT AND TEST METHOD FOR SWITCHING SYSTEM
Enclosed are:

1. [X] 14 pages of specification, claims, abstract
2. [X] 5 sheets of FORMAL drawing.
3. [X] 2 pages of newly executed Declaration & Power of Attorney (original).
4. [X] Priority Claimed.
5. [ ] Small Entity Statement.
6. [ ] Information Disclosure Statement, Form PTO-1449 and reference.
7. [X] Assignment Papers for LG Information & Communications, Ltd. (cover sheet, assignment & assignment fee).
8. [X] Certified copy of Korean Patent Application No. 38783/1998 filed September 18, 1998..
9. [X] Two (2) return postcards.
   [X] Stamp & Return with Courier.
   [X] Prepaid Postcard-Stamped Filing Date & Returned with Unofficial Serial Number.

[X] Authorization under 37 C.F.R. §1.136(a)(3).
[ ] Other:

CLAIMS AS FILED					
For	No. Filed		No. Extra	Rate	Fee
Total Claims	15	- 20	0	X $18.00	$0.00
Indep. Claims	3	- 3	0	X $78.00	$0.00
Multiple Dependent Claims (If applicable)				X $260.00	$0.00
				BASIC FEE	$760.00
				TOTAL FILING FEE	$760.00

[ ] This is a Continuation-in-part (CIP) of prior application No: _____ filed _____. Incorporation By Reference-The entire disclosure of the prior application is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
[ ] Amend the specification by inserting before the first line the sentence:
--This application is a continuation-in-part of Application Serial No. _____ filed _____.--
[X] A check in the amount of $760.00 (Check #7635) is attached.
[ ] Please charge my Deposit Account No. 16-0607 in the amount of $___. A duplicate copy of this sheet is enclosed.
[X] The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 16-0607. A duplicate copy is enclosed.
[X] Any additional filing fees required under 37 C.F.R. 1.16.
[X] The Commissioner is hereby authorized to charge payment of following fees during the pendency of this application or credit any overpayment to Deposit Account No. 16-0607. A duplicate copy of this sheet is enclosed.
[X] Any patent application processing fees under 37 C.F.R. 1.17.
[X] Any filing fees under 37 C.F.R. 1.16 for presentation of extra claims.

FLESHNER & KIM

Daniel Y.J. Kim
Registration No. 36,186

Correspondence Address Below:
P.O. Box 221200
Chantilly, VA 20153-1200
(703) 502-9440 FAX
Date: September 14, 1999

PATH MANAGEMENT AND TEST METHOD FOR SWITCHING SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a switching system, and in particular to a path management and test method for a switching system having a dual active structure.

2. Description of the Background Art

Figure 1 is a block diagram illustrating a conventional switching system. As shown therein, the conventional switching system includes a central subsystem 100 for performing an operator matching function for a switch operation and maintenance and storing a certain program, an interconnection subsystem 200 for performing a switching function for providing a switch number interpretation function and a communication path between switching subsystems, and a plurality of switching subsystems 300 for performing a subscriber and interconnection line matching and switching function.

Each subsystem of the switching system includes a processor. An OMP(Operating and Maintenance Processor) which is a main processor of the central subsystem 100, a SNP(Switching Network Processor) which is a main processor of the interconnection subsystem 200, and a SSP(Switching Subsystem Processor) which is a main processor of the switching subsystem 300 perform a request and response operation between processors.

In addition, the path(PCM path) through which voice or data are

transmitted is provided for each device apparatus(subscribver board, interconnection line board, various switch boards, etc). In order to implement the above-described operation, the subsystem includes a device controller(not shown) which is a low level processor for controlling the device.

In the above-described conventional switching system, in order to implement a service stability, the hardware board is constructed in a dual board system for effectively transmitting data.

Therefore, an active path through which data are transmitted is set at an initial stage based on the dual board system. In the case that an error occurs in the active path, there is provided a switching system of an active/standby in which a path is automatically or manually switched to a separately provided standby path.

In the switching system of the active/standby structure, a PCM(Pulse Code Modulation) data path is formed in the active path. The thusly formed data path is switched to the standby path at the time of a dual switch by an operator or when an error occurs in the active path(board).

When a switching function is performed for the standby path, in order to implement a continuity of the services, a maintenance is required for the standby path. In the switching system of an existing active/standby structure, it is impossible to test the standby path. Only the active path is tested using a switching function to the active/standby path based on an operator's request. In addition, there is a limit in the teat path interval with respect to the active path.

In a switching system having a dual active structure which is developed to provide a more stable service compared to the switching system of the active/standby structure, a certain path is set as an active path, and the data

inputted from a transmission side device is transmitted via two paths.

Therefore, at the board side, the standby path does not separately exist. However, at the receiving side device, since a data from one board is inputted, a transmission path of a valid data which reaches the receiving side device may become an active path, and the opposite path may become a standby path.

In the switching system of the dual active structure, in order to enhance a continuity of the services, a previous test function is required for the standby path. Since the active and standby paths are not previously set, it is difficult to separate each path. Therefore, it is impossible to effectively manage each path, and a certain continuity and reliability of the system are not implemented.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a path management method for a switching system which is capable of periodically checking a path state of each hardware board in a switching system of a dual active structure, managing a database and informing the changed state of the hardware board to an operator.

It is another object of the present invention to provide a standby path setting method which is capable of searching an actual active path at the current point based on the database.

It is another object of the present invention to provide a path test method for a switching system capable of implementing a path test for the entire intervals or a certain interval with respect to the active and standby paths.

To achieve the above objects, there is provided a path management and

testing method for a switching system which includes the steps of a step, in which the device controller checks a valid path and state change for each board, for forming a database using a main processor, a step for searching the database and confirming a standby path, and a step for performing a path test for the entire interval or a certain interval with respect to the active or standby path wherein the switching system which includes a plurality of devices formed in a dual active structure, a device controller for controlling the devices, and a main processor.

Additional advantages, objects and features of the invention will become more apparent from the description which follows.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:

Figure 1 is a block diagram illustrating the construction of a conventional switching system;

Figure 2 is a flow chart illustrating a path management and test method for a switching system according to the present invention;

Figure 3 is a flow chart illustrating a path state database formation according to the present invention;

Figure 4 is a view illustrating a hardware board construction for a switching system of a dual active structure for explaining a path setting method according to the present invention; and

Figure 5 is a flow chart illustrating a path test operation according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The embodiments of the present invention will be explained with reference to the accompanying drawings.

The construction of the switching system according to the present invention is the same as the construction of Figure 1. Figure 2 is a flow chart illustrating a path management and test operation for a switching system according to the present invention, Figure 3 is a flow chart illustrating a path state database formation, Figure 4 is a block diagram illustrating an example of a switch network construction for a switching system which is implemented by a dual active system for explaining a method for searching an actual active path, and Figure 5 is a flow chart illustrating a test operation with respect to an active or standby path.

The path management and test method for a switching system according to the present invention will be explained with reference to Figure 2 through Figure 5.

As shown in Figure 2, the path management and test method for a switching system according to the present invention includes a step S10 for forming a database for a state of each board, a step S20 for judging whether a path test request is inputted, a step S30 for searching an active path by searching a database when a path test request is inputted, a step S40 for setting a complete reverse path of the active path to a standby path, and a step S50 for performing a

test operation with respect to the active or standby path.

As shown in Figure 3, the database formation step S10 for each board state will be explained.

In the database formation step S10, a device controller checks a valid path state of each board which forms the switch network in an initial state step S11, and the checked state is outputted to the main processor, and the main processor forms a database for the checked state in Step S12.

After a certain time in Step S13, the device controller checks the state of each board in Step S14 is such a manner that a cycle having a certain period is registered for checking a time-based state change of a device, namely, a path change or a certain error. For example, in the present invention, a period is set as 100msec, and the state change of the device is checked at every 10msec.

Therefore, after a time of 100msec, it is judged whether the state change of the device occurs in Step S15. If there is a state change, the changed state is informed of the main processor, and the data with respect to the current device state is corrected by the main processor. If there is not a state change as a result of Step S15, the routine is returned to Step S13.

The path state of the current device managed by the database may be outputted to an operator.

Here, in the database, it is possible to check the valid side of a bidirectional path based on the unit of each board. In addition, the database is formed to check the states of the board and path.

In a state that the state of the device is periodically managed, a test request is inputted with respect to the active or standby path by an operator in Step S20, an actual active path is first checked in Step S30.

With reference to Figure 4, the method for searching an actual active path will be explained when a communication is performed between two switching sub-systems.

As shown in Figure 4, the construction for implementing a communication from a first switching subsystem 300-1 to a second switching subsystem 300-2 via an interconnection subsystem 200 includes MDXCs(Multiplexer & Demultiplexer Card) 11A, 11B, 12A, 12B, TSICs(Time Slot Interchange Card) 21A, 21B, 22A, and 22B, TLNCs(Time Switch & Link Card) 31A, 31B, 32A, and 32B, SLNCs(Space Switch & Link card) 41A, 41B, 42A and 42B, and SSWCs(Space Switch Card) 50A and 50B which are connected at a transmission side and receiving side, respectively, in pair. Figure 4 illustrates an example that A-side boards form an active path in the constructions of various switch networks.

The MDXC 11A, 11B, 12A and 12B are directly matched with the transmission side or receiving side terminal such as a subscriber or interconnection line, etc. The data inputted from the transmission side terminal are all applied to the MDXC-A/B 11A and 11B of the first subsystem 300-1, and the MDXC-A 12A of the second subsystem 300-2 operates in the active mode by the data outputted from the receiving side terminal. Namely, the operation is performed at 1:2 based on the MDXC 11A and 11B at the transmission side terminal, and the operation is performed at 1:1 based on the receiving side terminal of the MDXC 12A and 12B.

In other words, the operation is performed at 1:2 in the direction from the data transmitting side to the data receiving side, and the operation is performed at 1:1 in the direction from the data receiving side to the data transmitting side. Namely, the active path is searched in the sequence of the MDXC 12A, TSIC 22A

and TLNC 32A of the second subsystem 300-2.

Therefore, it is possible to search an actual active path as shown by the full line of the drawings.

In the next step, the reverse path of the active path is set as a standby path in Step S40.

When the active and standby paths are set, a test is performed with respect to a certain path based on a request of the operator in Step S50. The above-described operation will be explained in more detail with reference to Figure 5.

As shown therein, various parameters which are needed for a path test are received from the operator in Step S51. In the present invention, various parameters are used as follows. SUB1 indicates a subsystem in which a board is mounted for inserting a test pattern data. PBA1 indicates a board for inserting a test pattern data. LINK1 indicates a link number in the switching subsystem. SUB2 indicates a subsystem in which a board is mounted for extracting a test pattern data. PBA2 indicates a board for extracting a test pattern data. LINK2 indicates a link number in the switching subsystem. SIDE is a parameter for indicating whether the path to be tested corresponds to an active path ACT and a standby path SBY, and whether two paths NORM are tested, or whether a multiple channel test MULTI is performed with respect to a standby path. TYPE indicates whether a test is performed with respect to a single direction path ONEWAY or a bidirectional test LPBK is performed based on a loop-back test. DATA is a pattern data used for a test. CNTR indicates the number of repeated tests.

After the parameters which are needed for the path test are inputted, the

test-requested path is confirmed based on the inputted parameters in Step S52, and the switching path which corresponds to the test path is formed in Step S53.

In addition, a test pattern data is inserted into the input side board PBA1 in Step S54, and the test pattern data is extracted from the output side board PBA1 in Step S55.

The interval-based path test is performed in Steps S51 through S56. The test is performed by variously changing the input and output side boards PBA1 and PBA2, so that it is possible to accurately locate the interval in which an error occurred.

After Step S56 is performed, the test result is outputted, and the parameters PERD and CNTR are checked, and Steps S54 through S58 are performed as many as the operation periods PERD and the operation numbers CNTR, and then the test operation is completed.

As described above, in the switching system of the dual active structure according to the present invention, a path state of each board is checked, and an actual active path is searched. Thereafter, a standby path is set, and it is possible to test a path for the entire intervals or an interval-based path with respect to the active or standby path, so that a continuity and reliability of the service are enhanced, and it is possible to implement an easier system maintenance.

Although the preferred embodiment of the present invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as recited in the accompanying claims.

What is claimed is:

1. A switching system which includes a plurality of devices formed in a dual active structure, a device controller for controlling the devices, and a main processor, a path management and testing method for a switching system, comprising:

a step, in which the device controller checks a valid path and state change for each board, for forming a database using a main processor;

a step for searching the database and confirming a standby path; and

a step for performing a path test for the entire interval or a certain interval with respect to the active or standby path.

2. The method of claim 1, wherein said step for forming a path state database for each board includes:

a step in which the device controller reads a valid path for each board to a device at an initial state stage and informs a main processor of the read path;

a step in which the main processor forms a database using the read path;

a step for checking a device-based state change at a certain period; and

a step for editing the database based on the state change.

3. The method of claim 1, wherein in said step for checking the active path, in which an active path to the matched last receiving board is checked by the receiving side terminal, and an active path is checked in the reverse direction of the data transmission direction, and the entire active paths are searched by checking the switching path of the boards connected with the active path.

4. The method of claim 1, wherein in said standby path setting step, in the case that a certain path is set as an active path which is different from the current path by checking the valid path for each board with respect to the standby path which is set as the reverse path of the active path, the set path is changed.

5. The method of claim 1, wherein said path test step includes:

a step for receiving a parameter value used for a path test;

a step for forming a test path based on the parameter value;

a step for inserting a test pattern data into an input side device;

a step for extracting a test pattern data from an output side device; and

a step for judging an error with respect to the test path interval by comparing an input data and an extraction data.

6. The method of claim 5, further comprising a step for setting the number of repetitions and setting a period for thereby repeatedly performing the test.

7. The method of claim 5, further comprising a step for performing an interval-based path test when the input data and the extracted data are different and searching an error interval.

8. The method of claim 5, wherein said parameter value indicates the kind of a test path and a test type, a board for inserting or extracting a test pattern data, a subsystem in which the board is mounted, a link number in the subsystem,

and a pattern data used for the test.

9. The method of claim 8, wherein said parameter value includes a value which indicates a test repetition period and repetition number.

10. In a switching system of a dual active structure, an actual active path judging method, comprising:

checking an active path formed in a direction of a matched last receiving board at a receiving side terminal;

checking an active path in the reverse direction of a data transmission direction; and

searching an entire active path by checking a switching path of the board connected to the active path.

11. In a switching system of a dual active structure, a standby path test method, comprising:

a step for checking an active path formed in a direction of a matched last receiving board at a receiving side terminal, checking an active path in the reverse direction of a data transmission direction, and searching an entire active path by checking a switching path of the board connected to the active path;

a step for setting a reverse path of the active path as a standby path; and

a step for performing a path test with respect to the set standby path.

12. The method of claim 11, wherein said path test step includes:

a step for receiving a certain parameter value needed for a path test;

a step for forming a switching path based on the set standby path;

a step for inserting a test pattern data into the input side device;

a step for extracting a test patten data from the output side device;

a step for judging whether there is an error in the standby path based on a comparison result with respect to the input data and the extraction data; and

a step for searching an error interval by performing an inter-based path test in the case that the input data and the extracted data are not same.

13. The method of claim 12, further comprising a step for repeatedly performing a test by setting the number of repetitions and period.

14. The method of claim 12, wherein said parameter value indicates a test type, a board for inserting or extracting a test pattern data, a subsystem for mounting the board, a link number in the subsystem, and a pattern data used for the test.

15. The method of claim 14, wherein said parameter value indicates a test repetition period and repetition number.

ABSTRACT OF THE DISCLOSURE

The present invention relates to a switching system, and in particular to a path management method for a switching system which is capable of periodically checking a path state of each hardware board in a switching system of a dual active structure, managing the checked state based on a database, so that an operator recognizes a change in the states of the hardware boards. In addition, the present invention provided a standby path capable of searching an actual active path at the current point based on the database. A path test method for a switching system is provided for thereby implementing a path test for an entire interval or a certain interval with respect to the active and standby paths. Therefore, in the present invention, it is possible to enhance a continuity and reliability of a service and implement an easier maintenance of the system.

FIG. 1
BACKGROUND ART

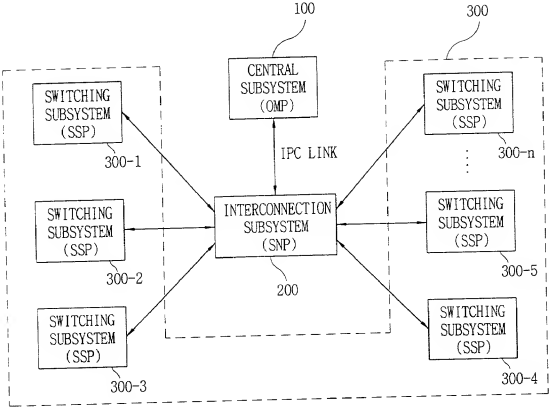


FIG. 2

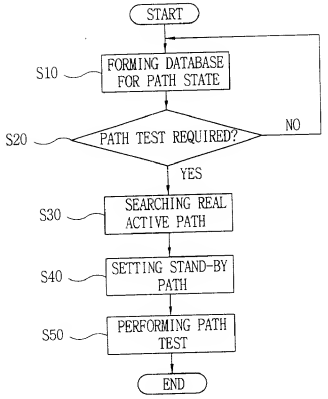


FIG. 3

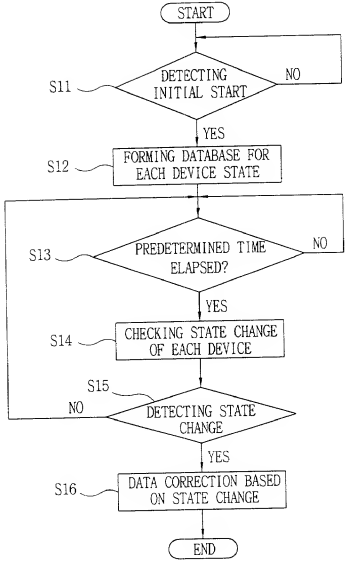

START
S11
DETECTING INITIAL START
NO
YES
S12
FORMING DATABASE FOR EACH DEVICE STATE
S13
PREDETERMINED TIME ELAPSED?
NO
YES
S14
CHECKING STATE CHANGE OF EACH DEVICE
S15
NO
DETECTING STATE CHANGE
YES
S16
DATA CORRECTION BASED ON STATE CHANGE
END

FIG. 4

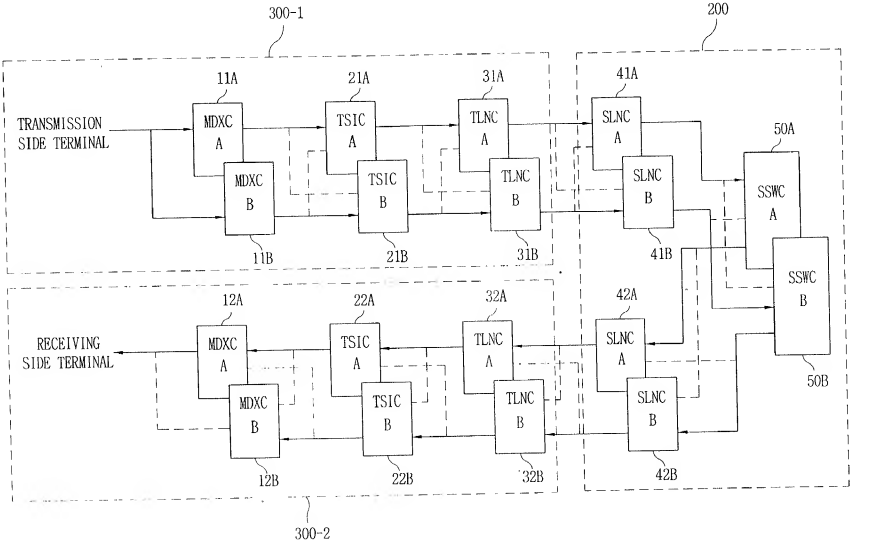
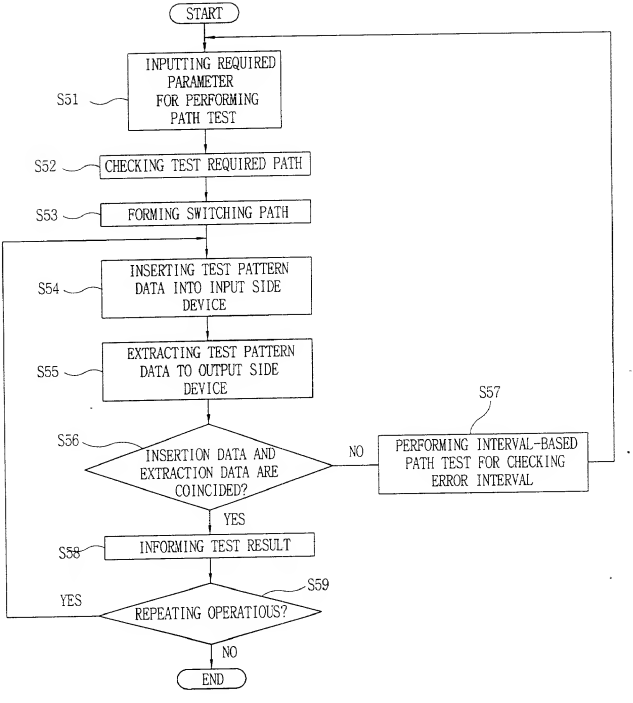

300-1
200
11A
21A
31A
41A
TRANSMISSION SIDE TERMINAL
MDXC A
TSIC A
TLNC A
SLNC A
50A
MDXC B
TSIC B
TLNC B
SLNC B
SSWC A
SSWC B
11B
21B
31B
41B
50B
12A
22A
32A
42A
RECEIVING SIDE TERMINAL
MDXC A
TSIC A
TLNC A
SLNC A
MDXC B
TSIC B
TLNC B
SLNC B
12B
22B
32B
42B
300-2

FIG. 5


START
INPUTTING REQUIRED PARAMETER FOR PERFORMING PATH TEST
S51
CHECKING TEST REQUIRED PATH
S52
FORMING SWITCHING PATH
S53
INSERTING TEST PATTERN DATA INTO INPUT SIDE DEVICE
S54
EXTRACTING TEST PATTERN DATA TO OUTPUT SIDE DEVICE
S55
INSERTION DATA AND EXTRACTION DATA ARE COINCIDED?
S56
NO
PERFORMING INTERVAL-BASED PATH TEST FOR CHECKING ERROR INTERVAL
S57
YES
INFORMING TEST RESULT
S58
REPEATING OPERATIOUS?
S59
YES
NO
END

Docket No.: _____

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter claimed and for which a patent is sought on the invention entitled _____

PATH MANAGEMENT AND TEST METHOD FOR SWITCHING SYSTEM

_____, the specification of which

[X] is attached hereto [ ] was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is known to me to be material to patentability in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority or provisional application benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate, or provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate, or provisional application(s) having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s) or U.S. Provisional Application(s):			Priority Claimed	
Number	Country	Day/Month/Year	Yes	No
38783/1998	Korea	18/09/1998	x	

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U. S. Application(s): Serial No.	Filing Date	Status: Patented, Pending, Abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) and/or agent(s):Daniel Y.J. Kim, Registration No. 36,186 and Mark L. Fleshner, Registration No. 34,596; Carl R. Wesolowski, Registration No. 40,372, John C. Eisenhart, Registration No. 38,128, and Rene A. Vazquez, Registration No. 38,647; Michael J. Cornelison, Registration No. 40,395; and Stuart I. Smith , Registration No. 42,159, all of

FLESHNER & KIM
P.O. Box 221200
Chantilly, Virginia 20153-1200

with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and all further correspondence should be addressed to them

****

Full name of solo or first inventor: YEO NAM SOO

Inventor's signature: Yeo Nam Soo Date: 1999. 9. 6

Residence: Ahnsan, Korea

Citizenship: Republic of Korea

Post Office Address: 659-2302, Il-Dong, Ahnsan, Kyungki-Do, Korea

****

Full name of solo or first inventor: KIM IN TAE

Inventor's signature: Kim In Tae Date: 1999. 9. 6

Residence: Anyang, Korea

Citizenship: Republic of Korea

Post Office Address: Mokryun Apt. 201-1005, 1052, Hogye-Dong, Dongan-Ku, Anyang, Kyungki-Do, Korea

****

Full name of joint inventor(s): KIM JONG HO

Inventor's signature: Kim Jong Ho Date: 1999. 9. 6

Residence: Anyang, Korea

Citizenship: Republic of Korea

Post Office Address: Chowon Booyung Apt. 703-1101, Pyungchon-Dong, Dongan-Ku, Anyang, Kyungki-Do, Korea

****

Full name of joint inventor(s): HWANG In HWAN

Inventor's signature: Hwang in hwan Date: 1999. 9. 6

Residence: Inchon, Korea

Citizenship: Republic of Korea

Post Office Address: Sungdoo Villa 1-202, 395-13, Jooan 1-Dong, Nam-Ku, Inchon, Korea